The Development of 40 Gb/s Limiting-Distributed Modulator Drivers in InP HBTs

Mark Yu, Zhihao Lao[1], Shing Lee, Vesna Radisic[2], Muliang Xu[3], Vincent Ho[2], Keith Guinn[1], and K.C. Wang

Advanced Product Development Center, Opnext, Inc., Thousand Oaks, CA, 91362.

Abstract — **The development of monolithic modulator drivers designed into InP SHBTs technologies for 40-Gb/s optical communications is presented. The drivers consist of a differential limiting pre-driver and a differential distributed post-amplifier to achieve enough gain-bandwidth product, and feature cross-point control and output amplitude adjustments to ensure sufficient output extinction ratio. The drivers have achieved output swings of 2.6 Vp-p at each side with a 0.5 Vp-p single-sided input, and consume 1.72 W power.**

I. Introduction

The typical transmitter of a light-wave communication system consists of a time-division multiplexer, and a driver that amplifies the high-speed electrical signal for direct modulation to a CW-laser diode or external modulation to an optical modulator. At the bit rate of 40-Gb/s, the electroabsorption modulators (EAM) are normally used for very-short range (VSR) to short range (SR) transmission, and the EAM must operate at high-speed and requires a minimum drive voltage of 2.3 Vp-p to ensure sufficient extinction ratio.

For 40-Gb/s driver applications, three popular topologies of modulator drivers are normally adopted [1]-[7]. Conventional distributed amplifiers exhibit exceptional broadband performance, good S_{11} & S_{22}, and low power dissipation, but they suffer from low voltage gain, an external bias-T requirement, limited control functionalities, and sensitive to bias condition. Since most of these control functions are driven with push-pull operation, the single-ended topology is inappropriate to incorporate these features. Differential lumped limiting amplifiers can provide not only these functions, but they also exhibit low power dissipation, superior gain performance, reduced time-jitter, and standard current-mode logic (CML) interface at both input and output. Nevertheless, the drawback of this topology is its poor S_{22} performance due to its high capacitance characteristic of the large switching pair mismatched to 50-Ω loads, which results in limited bandwidth. Therefore, incorporating the limiting amplifier with a distributed amplifier improves the bandwidth characteristics and provides sufficient gain-bandwidth product. This topology was first demonstrated by Miyashita *et al.* [4] for a 10-Gb/s modulator driver.

This paper provides the advances in the development of the 40 Gb/s modulator driver designed into 1 μm InP SHBT process as compared with previously reported results in 0.15 μm GaAs pHEMT process with 4 W power dissipation at –5.6 V power supply [5], and 1 um InP SHBT with 2.4 Vp-p output swings for consuming 1.8 W at –5.0 V supply [7]. The drivers are capable of delivering 2.6 Vp-p swings at each output with a 0.5 Vp-p single-sided input signal. It consumes 1.72 W power at a standard power supply of –5.2 V.

II. Circuit Design

A block diagram of the limiting-distributed driver is shown in Fig. 1. It is composed of a single-stage limiting amplifier as the pre-driver and a distributed post-amplifier with five gain cells. A variable cross-point control (XPC) is included at the inter-stage so that the variation of the crossing point resulted in the change of external voltage control would not affect the bias levels at the input and output of the driver. The limiting amplifier as shown in Fig. 2 consists of two pairs of emitter followers with level-shifting diodes served for impedance transformation and providing proper dc-bias level for the following cascode differential pair. The input on-chip 50-Ω resistors were

[1] Zhihao Lao and Keith Guinn were with Opnext, Inc., Thousand Oaks, CA 91360. They are now with HRL Laboratories, LLC, Malibu, CA 90265

[2] Vesna Radisic and Vincent Ho were with Opnext, Inc., Thousand Oaks, CA 91360. They are now with Northrop Grumman Corporation, Space and Electronics, Redondo Beach, CA 90278

[3] Muliang Xu was with Opnext, Inc., Thousand Oaks, CA 91360. He is now with RF Integrated Corporation, Irvine, CA 92618

0-7803-7694-3/03/$17.00 © 2003 IEEE

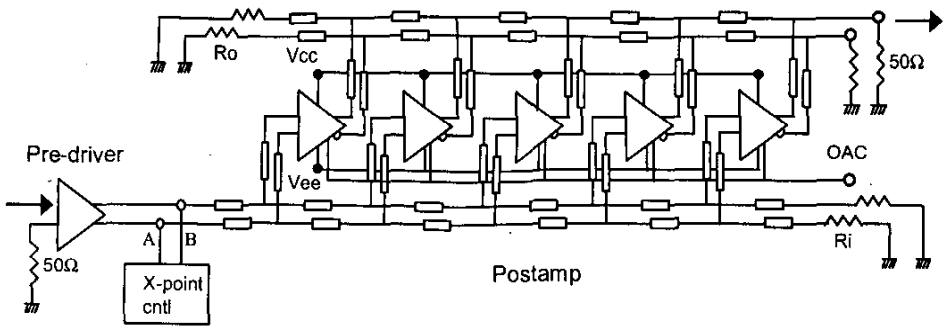

Fig. 1. Block diagram of the limiting-distributed modulator driver

used to match the data with the source impedance, and the cascode differential inverters were adopted to provide higher bandwidth due to reduced Miller capacitance and better isolation from the output. Both the emitter followers and the amplification stage were biased at the peak of f_T for its optimum performance. The output load resistors of 50-Ω were used to provide the impedance match with the input termination resistors, Ri, of the following distributed amplifier. The source current of 20 mA produces an output voltage swing of 450 mVp-p per side, which, in turn, drives each of the gain-cell of the distributed amplifier.

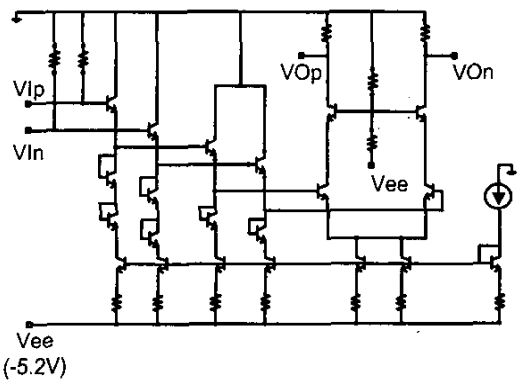

Fig. 2. Schematic diagram of the pre-driver

To ensure a better performance of the driver, the driver also includes a variable cross point control (XPC) and an output amplitude control (OAC), which is distributed in all the gain cells of the distributed amplifier. The XPC circuit is a simple differential pair. As a difference voltage is applied to the input of the control, it results in an offset voltage between port A and B (shown in Fig. 1), changing the dc characteristics at the inter-stage, and thus varying the cross-point of the output signal. The output amplitude control was designed by simply varying the current source of each gain-cell, and thus the voltage magnitude may be adjusted.

In the design of the post-amplifier, for each gain-cell single emitter follower was used to lower the total power dissipation. Together with three level-shifting diodes drives an open-collector cascode pair. The output load of the distributed amplifier, Ro=40-Ω, was used to optimize the gain flatness. Each gain cell delivering 25 mA through an effective load of about 22-Ω is designed to provide an output voltage swings of 2.7 Vp-p at each side. The output transmission lines and impedance were carefully designed to avoid possible on-chip ringing, which could be induced by the highly inductive transmission lines coupled with the large capacitance characteristics of the open-collector differential pairs.

The drivers were fabricated by Global Communication Semiconductors Corporation[4] on a 4" semi-insulating InP substrate and employed 1 μm emitter-length InP SHBT technology, which has f_T of greater than 160 GHz and current gain (β) of over 30. The die dimension is 2.5x1.4 mm^2 and was thinned down to 125 μm substrate thickness to ensure proper heat dissipation. The die photograph of the limiting distributed driver is shown in Fig. 3.

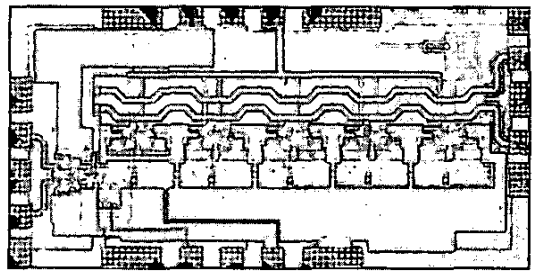

Fig. 3. Die photograph of the EAM driver IC.

III. MEASURED RESULTS

The circuit performance was measured by using 50-Ω on-wafer probes. The driver exhibits an overall large signal gain of 17 dB per side and consumes only 1.72 W using single power supply of –5.2 V. The well-opened eye diagram is shown in Fig. 4, where the differential data inputs at 40-Gb/s with a pseudorandom bit sequence (PRBS) of the length 2^{31}-1 was applied for the IC driving 50-Ω loads. A voltage swing of 2.6 Vp-p (measured at mean 1 and mean 0) was obtained at each output with a single-sided input signal of 0.5 Vp-p. The rise and fall time at 20-80% was less than 9 ps, and the peak-to-peak time-jitter was about 8 ps. A cross-point variation of 20-80% was also obtained.

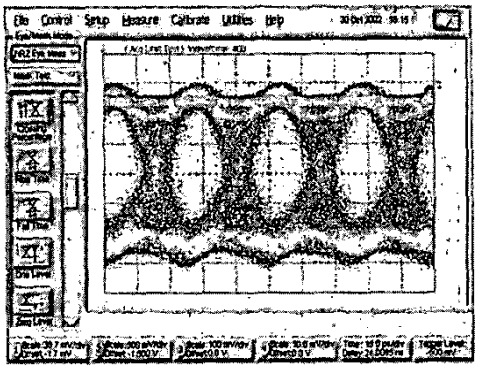

Fig. 4. Measured 40-Gb/s eye diagram with 0.5 Vp-p single-sided input.

V. CONCLUSION

The development of our second-generation modulator drivers for 40-Gb/s optical fiber links using 1 μm emitter-length InP SHBT process has been presented. The limiting distributed driver featured differential input and output delivers 2.6 Vp-p voltage swings at each side with less than 9 ps rise/fall time for 0.5 Vp-p single-sided input. The power consumption was 1.72 W using standard power supply of -5.2 V. As compared with the previously reported 4 W power consumption and 12 ps rise/fall time in 0.15 μm GaAs pHEMT process, and 1.8 W at 2.4 Vp-p in InP HBT reported by Radisic *et al.*, these results show tremendous progress in the driver development. The addition of cross-point adjustment and the amplitude control also provides improved extinction ratio for the EA modulator.

REFERENCES

[1] R.S. Virk, E. Camargo, R. Hajji, S. Parker, R. Benelbar, S. Notomi, and H. Ohnishi, "40-GHz MMICs for optical modulator driver applications," *IEEE MTT-S Digest,* pp. 91-94, 2002.

[2] Y. Baeyens, R. Pullela, J.P. Mattia, H.S. Tsai, and Y.K. Chen, "A 74-GHz bandwidth InAlAs/InGaAs-InP HBT distributed amplifier with 13-dB gain," *IEEE Microwave and Guided Wave Letters,* vol. 9, No. 11, pp. 461-463, 1999.

[3] Z. Lao, A. Thiede, U. Nowotny, H. Lienhart, V. Hurm, M. Schlechtweg, J. Hornung, W. Bronner, K. Kohler, A. Hulsmann, B. Raynor, and T. Jakobus, "40-Gb/s high-power modulator driver IC for lightwave communication systems," *IEEE J. Solid-State Circuits,* vol. 33, pp. 1520-1526, 1998.

[4] M. Miyashita, K. Yamamoto, K. Andoh, N. Okada, K. Motoshima, and A. Takemoto, "A 10-Gb/s AlGaAs/InGaAs p-HEMT distributed EA driver with a D-flip-flop for optical fiber links," *IEEE GaAs Digest,* pp. 205-208, 2000.

[5] M. Yu, Z. Lao, S. Lee, M. Xu, V. Ho, V. Radisic, K. Guinn, and K.C. Wang, "40-Gb/s low-voltage distributed limiting drivers for optical modulators," submitted to *IEE Electronics Letters.*

[6] D.S. McPherson *et al.*, "A 3-V fully differential distributed limiting driver for 40 Gb/s optical transmission systems," *IEEE GaAs IC Symposium Digest*, pp. 95-98, 2002.

[7] V. Radisic, M. Yu, Z. Lao, V. Ho, M. Xu, K. Guinn, and K.C. Wang, "40 Gb/s differential traveling wave modulator driver," submitted to *IEEE Microwave and Guided Wave Letters.*